UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,478	08/13/2001	Warren M. Farnworth	3401.5US (97-710.5)	7943

24247 7590 11/05/2002

TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/928,478	Applicant(s) FARNWORTH ET AL.
	Examiner John B. Vigushin	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continuing Application

1. The instant Application is a continuation of US Application Serial No. 09/651,460, filed August 30, 2000 (now US Pat. 6,295,209), which is a continuation of US Application Serial No. 09/464,992, filed December 16, 1999 (now US Pat. 6,144,560), which is a continuation of US Application Serial No. 09/296,952, filed April 22, 1999 (now US Pat. 6,091,606), which is a continuation of US Application Serial No. 09/002,063, filed December 31, 1997 (now US Pat. 5,940,277). The Examiner has reviewed the prior art cited or relied upon in the above-mentioned parent Applications as required by the MPEP § 2001.06(b).

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Akram et al. (US 6,072,236)

Lee et al. (US 5,386,087)

Yunoki et al. (US 5,236,372)

Kniese et al. (US 4,806,103)

Dines (US 4,303,291)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 5-9, 12, 17, 18, 20 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Akram et al.

As to Claim 1, Akram et al. discloses, in Figs. 6-8, at least one contact pad 116 positioned on a surface of semiconductor device 12 adjacent an edge thereof; a layer 20 comprising dielectric material (i.e., a ceramic material: col.5: 47-51), the layer 20 having a notch 22 formed therein which exposes at least a portion of the at least one contact pad 116 (col.6: 32-39).

As to Claim 5, Akram et al. further discloses that layer 20 covers substantially all of the semiconductor device surface (Figs. 6-8).

As to Claim 6, Akram et al. further discloses that notch 22 substantially surrounds the at least one contact pad 116 (Fig. 6).

As to Claim 7, Akram et al. further discloses a plurality of contact pads 116 (Fig. 6).

As to Claim 8, Akram et al. further discloses that at least some of contact pads 116 are located adjacent the edge (Fig. 6).

As to Claim 9, Akram et al. further discloses that layer 20 includes regions extending laterally between adjacent contact pads 116 of the at least some contact pads 116 (Fig. 6).

As to Claim 12, Akram et al. discloses a substantially planar member 20 comprising dielectric material (i.e., ceramic material: col.5: 47-51); at least one notch 22 formed adjacent an edge of substantially planar member 20; at least one notch 22 configured to expose at least a portion of a corresponding contact pad 116 of the semiconductor device 12 upon positioning the protective layer (i.e., substantially planar member 20) over a surface of semiconductor device 12 (col.6: 32-39).

As to Claim 17, Akram et al. further discloses a plurality of notches 22 located along the edge (Fig. 6).

As to Claim 18, Akram et al. further discloses that substantially planar member 20 is configured to substantially cover a surface of semiconductor device 12 upon assembly therewith (Fig. 6).

As to Claim 20, Akram et al. further discloses that the notches each comprise an aperture 22 in communication with a trench 122 formed in the edge (col.6: 39-42); hence, at least one notch is formed in the edge (Figs. 6 and 7).

As to Claim 21, Akram et al. further discloses that at least one notch 22 is configured to substantially surround the corresponding contact pad upon assembly of the protective layer (i.e., substantially planar member 20) with semiconductor device 12 (Fig. 6).

5. Claims 12-14 and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yunoki et al.

As to Claim 12, Yunoki et al. discloses a substantially planar member 34 comprising a dielectric material (col.5: 23-25); at least one notch 35 formed adjacent an edge 35a of substantially planar member 34 (col.5: 63-68), the at least one notch 35 configured to expose at least a portion of a corresponding contact pad 32, 33 "*upon positioning the protective layer over a surface of a semiconductor device*" (Italic emphasis by the Examiner). *Examiner's Note*: The at least one notch of the protective layer (dielectric planar member) "being configured to expose at least a portion of a corresponding contact pad of the semiconductor device ***upon positioning*** the protective layer over a surface of the semiconductor device" (bold emphasis by the Examiner) is *intended use of the protective layer (planar member)* because the protective layer (planar member) is **not actually structurally positioned** on a semiconductor device surface in the claim language; i.e., there is no semiconductor device actually present in the *positively claimed* structure: Only the structure of the protective layer (planar member) alone is claimed. It has been held that a recitation with respect to the manner in which a claimed apparatus (in this case, the *protective layer* or *planar member*) is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus (i.e., the planar member 34 of Yunoki et al.) satisfying the **claimed structural limitations**. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

As to Claim 13, Yunoki et al. further discloses a bevel (inclined wall) along the edge 35a (Fig. 2; col.5: 63-col.6: 4).

As to Claim 14, Yunoki et al. further discloses at least one edge 35a of at least one notch 35 is beveled (Fig. 2; col.5: 63-col.6: 4).

As to Claim 18, Yunoki et al. further discloses that the substantially planar member 34 is configured to substantially cover a surface (i.e., connector portion 31) of a semiconductor device **upon assembly** therewith (Fig. 2; col.5: 23-25). [*Examiner's Note*: The phrase "upon assembly" indicates *intended use* of the planar member 34; i.e., there is no semiconductor device actually present in the *positively claimed* structure: Only the structure of the protective layer (planar member) alone is claimed. See Examiner's Note in the rejection of Claim 12, above].

As to Claim 19, Yunoki et al. further discloses that substantially planar member 34 is configured to cover only a portion of a surface of a semiconductor device adjacent an edge thereof (i.e., connector portion 31) proximate to which at least one contact pad 32, 33 is located **upon assembly** of the protective layer with the semiconductor device (Fig. 2; col.5: 23-25). [*Examiner's Note*: The phrase "upon assembly" indicates *intended use* of the protective layer (planar member 34); i.e., there is no semiconductor device actually present in the *positively claimed* structure: Only the structure of the protective layer (planar member) alone is claimed. See Examiner's Note in the rejection of Claim 12, above].

As to Claim 20, Yunoki et al. further discloses at least one notch 35 is formed in the edge (Fig. 2).

As to Claim 21, Yunoki et al. further discloses that at least one notch 35 is configured to substantially surround the corresponding pad 33 **upon assembly** of the protective layer with the semiconductor device. [*Examiner's Note*: The phrase "upon assembly" indicates *intended use* of the protective layer (planar member 34); i.e., there is no semiconductor device actually present in the *positively claimed* structure: Only the structure of the protective layer (planar member) alone is claimed. See Examiner's Note in the rejection of Claim 12, above].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 4 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yunoki et al.

As to Claim 1:

I. Yunoki et al. discloses at least one contact pad 32, 33; on a surface of circuit board 30 adjacent an edge 31 thereof; a layer 34 comprising dielectric material on at least a portion of the surface, the layer 34 having a notch 35 formed therein which exposes at least a portion of the at least one contact pad 32, 33 (col.5: 23-27).

II. Yunoki et al. does not indicate the functional circuitry or components on the circuit board or card 30.

III. However, Yunoki et al. discloses circuit boards or cards for mounting into system board connectors 10 for electronic devices (see Fig. 1; col.1: 6-15), and furthermore, cards such as SIMMs, DIMMs, controller cards, processor cards are notorious in the art as add-on circuit boards that have semiconductor chips mounted thereon for the above-mentioned memory, control, communication and processing functions to be provided on an electronic device or computer system board. Accordingly, these circuit cards are part of the *packaging* of the SIMMs, DIMMs, controllers, communication devices and processors which are, respectively, representative of the various types of *semiconductor devices, i.e., circuit-board-packaged devices having semiconductor chips mounted thereon*, that are notorious in the art, as mentioned above.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit card 30 of Yunoki et al. to be a SIMM, DIMM, controller or processor card--i.e., a *semiconductor device* 30--for use in the electronic device contemplated by Yunoki et al.

As to Claim 4, Yunoki et al. further discloses that notch 35 is tapered from a surface of layer 34 toward the surface of semiconductor device 30.

As to Claim 6, Yunoki et al. further discloses that notch 35 substantially surrounds at least one contact pad (i.e., contact pad 33: Fig 2).

As to Claim 7, Yunoki et al. further discloses a plurality of contact pads (i.e., pads 32 and 33: Fig. 2).

As to Claim 8, Yunoki et al. further discloses that at least some of the contact pads (i.e., pads 32) are located adjacent the edge (Fig. 2).

As to Claim 9, Yunoki et al. further discloses that layer 34 includes regions extending laterally between adjacent contact pads 32 of the at least some contact pads 32 (Fig. 2).

8. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yunoki et al. in view of Kniese et al.

As to Claims 2 and 3:

I. Yunoki et al. discloses all the limitations of base Claim 1 but does including a beveled taper of the lateral portions 35a layer 34 defining notch 35, but does not teach a beveled taper from a surface of layer 34 *toward the edge* of the semiconductor device circuit card 30.

II. Yunoki et al. discloses a staggered array of contact pads 32 and 33 to be inserted into a connector and contacted by connector members 21 and 22 (Figs. 4 and 5). Kniese et al. also discloses a staggered array of contact pads on a circuit card 12 (Figs. 2B,C) but discloses a dielectric rib structure 28 (Figs. 1 and 6) that exhibit beveled tapers 31 toward the edge of the circuit card 12 (Figs. 1 and 6) wherein the beveled tapers 31 facilitate the movement of the longer connector contacts 18 over the rib structure and onto the appropriate row of contacts of the circuit card 12.

III. Since both Yunoki et al. and Kniese et al. are both in the same art of inserting a circuit card into the connector of an electronic system, then the beveled taper structure of the dielectric rib structure of Kniese et al. would have been readily

recognized by Yunoki et al. as a useful structural feature for layer 34 to facilitate and properly direct the movement of connector contact members 22 over the portions of layer 34 closest to the edge of circuit card 30 and onto the contacts 33 of the circuit card 30 as it is inserted into connector 10.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the portion of layer 34 nearest the connector edge of card 30 in Yunoki et al. with the beveled taper taught by Kniese et al. in order to facilitate and properly direct the movement of the contact members of connector 10 over the dielectric layer 34 and onto the card contacts 33 during insertion of the card 30 into connector 10, in Yunoki et al., as taught by Kniese et al.

9. Claims 10, 11, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yunoki et al. as applied to claims 1 and 12 above, and further in view of Dines and Lee et al.

As to Claims 10, 11, 15 and 16:

I. Yunoki et al. discloses all the limitations of base Claims 1 and 12, respectively, and further teaches a dielectric (insulating) layer 34 for protecting the connector portion 31 of the semiconductor package circuit card 30 but is silent as to the dielectric material composition of the layer 34.

II. Dines teaches a circuit card with a dielectric layer 13 having notches 46 exposing contact pads 43, wherein the dielectric layer 13 is a photoimageable material which is developed and set by exposure to ultraviolet (UV) light (Fig. 2; col.3: 12-18 and 55-62).

III. Lee et al. further discloses that such a UV photoimageable layer is a photopolymer material which cross-links (sets) upon exposure to UV light (Fig. 1; col.3: 44-46).

IV. Since Yunoki et al. and Dines and Lee et al. all protect the circuit substrate with a planar member dielectric layer, and Yunoki et al. and Dines are both in the same art of attaching circuit cards to a system connector, and since Dines and Lee et al. teach a photoimageable polymer material for protecting the card surface, then the use of the photoimageable polymer material for protecting the circuit card surface, as taught by Dines and Lee et al. would have been readily recognized as a an effective insulating material for the dielectric layer 34 in Yunoki et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to specifically use the dielectric material taught by Dines and Lee et al. (i.e., the photoimageable polymer material) as the dielectric material 34 in Yunoki et al. in order to effectively apply a dielectric layer for protecting the connector portion 31 on the circuit card component 30 of the semiconductor package of Yunoki et al.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) The following references disclose a semiconductor device with a dielectric layer thereon, the layer having notches that expose semiconductor device contacts:

Chung et al. (US 5,909,122): Figs. 1 and 2; notches 162 and 163.

Siegel et al. (US 5,557,504): Figs. 1 and 2; notches 14 and 34.

Martin (US 5,412,247): Figs. 2 and 3; notches 54, 56, 58 and 60.

b) Rostoker et al. (US 5,729,894) discloses a BGA semiconductor package 200 having notches 260-267 in the resin molding 226 exposing chip carrier contacts 270-277 (Fig. 5; col.6: 5-11).

c) The following references disclose circuit cards with a dielectric layer thereon, the layer having notches that expose the card contacts:

Tanaka et al. (US 5,757,622): Figs. 2 and 3; notch 20.

Bare et al. (US 5,665,653) : Figs. 9 and 10.

Griffith et al. (US 4,298,237) : Fig. 3 ; notches 24a,b,c.

d) The following references disclose a semiconductor lead frame with molding material having a notch for exposing the leads at the edge(s):

Houdeau et al. (US 6,326,683 B1): Figs. 4 and 5; notch 17.

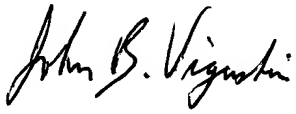
Marchisi (US 5,102,828): Figs. 3 and 4.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



John B. Vigushin
Examiner
Art Unit 2827

jbv
November 4, 2002